

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

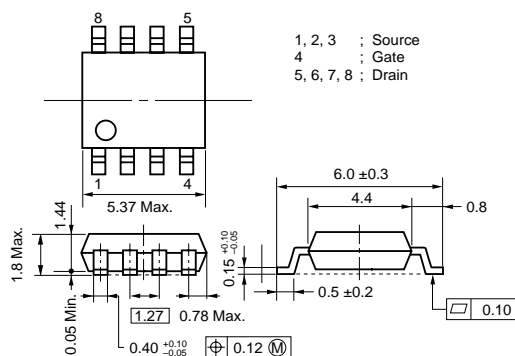
DESCRIPTION

The  $\mu$ PA1727 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Single chip type
- Low On-state Resistance
- ★  $R_{DS(on)1} = 14 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )
- ★  $R_{DS(on)2} = 17 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )
- ★  $R_{DS(on)3} = 19 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 4.0 \text{ V}$ ,  $I_D = 5.0 \text{ A}$ )
- Low  $C_{iss}$  :  $C_{iss} = 2400 \text{ pF}$  (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



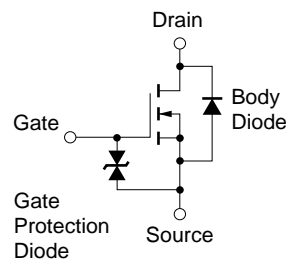
ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1727	Power SOP8

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 10$	A
Drain Current (Pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 40$	A
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	10	A
★ Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	200	mJ

EQUIVALENT CIRCUIT



Notes 1.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1 \%$

- ★ 2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
- 3. Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ }\Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

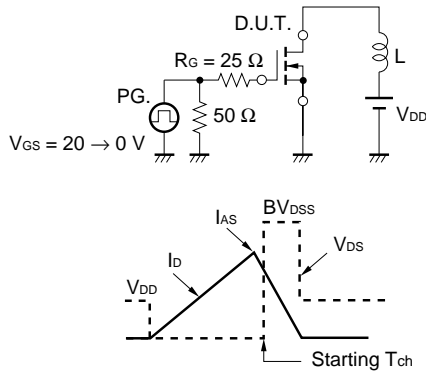
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

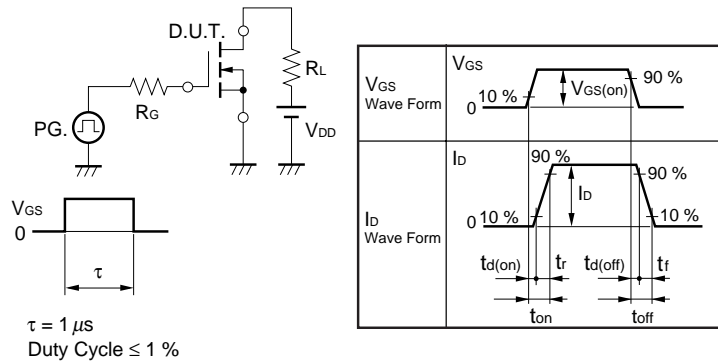
★ ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A		14	19	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A		17	22	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 5.0 A		19	25	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	8.0	14		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = 10 V		2400		pF
Output Capacitance	C <sub>oSS</sub>	V <sub>GS</sub> = 0 V		400		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>	f = 1 MHz		200		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 5.0 A		24		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		120		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 30 V		120		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		71		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 10 A		45		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 48 V		5.9		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		13		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		45		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs		84		nC

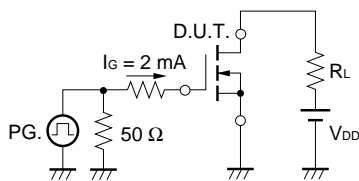
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



[MEMO]

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